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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,716	06/08/2000	Stephen V. Kosonocky	YO999-369	9798

7590 07/02/2004

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EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,716	KOSONOCKY, STEPHEN V.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6-20* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/19/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive filed 05/03/2004.

2. Claims 1-20 are pending in this application. Claims 1, 6, 13, and 20 are independent claims. This action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations cited in claim 2 must be shown or the feature(s) canceled from the claim(s), particularly the drawing must shown a structure of logic implementing according to the expression: ^(p(n) * C(n-1))*(p(n) + C(n-1)). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 18 is objected to because of the following informalities: a period (.) is required at the end of claim 18 line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. 5,905,667).

Re claim 1, Lee discloses an apparatus for use in summing at least two binary values (A and B) in Figure 4 comprising a binary adder circuit respective to a first binary value (A into MP11) a second binary value (B into MP12) and a carry value (C into MP13) and operative to generate a binary output value (SUM') representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having dynamic logic (col. 2 lines 29-32), without inversion of signals driving one or more dynamic nodes associated with the dynamic logic (no inverter or inverting mechanism is used in Figure 4, the CLKB signal without inversion is applied to N-MOS and P-MOS transistors in 41-44), for implement an exclusive OR function

(MP33, MP34 and col. 1 lines 41-45) that generates the binary output value (SUM) without one of a positive and a negative complementary version of the carry value (table 3 in col. 3 and col. 2 lines 65-68 and col. 3 lines 1-3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being obvious over Suzuki (U.S. 3,646,332) in view of Lee (U.S. 5,905,667).

Re claim 1, Suzuki discloses an apparatus for use in summing at least two binary values (binary A and B) in Figures 4 and 8 comprising a binary adder circuit (Figure 8) responsive to a first binary value (A), a second binary value (B), and a carry value (C or output of 5) and operative to generate a binary output value (S or sum or output of 12) representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic (no inverter or inverting mechanism is used in Figure 3), for implement an exclusive OR function (2' with Figure 4 as the logical structure of EXOR and col. 3 lines 16-20) that generates the binary output value without one of appositive and a negative complementary version of the carry value (only C is inputted to component 2' to compute the sum). Suzuki does not disclose the

adder is using a dynamic logic. However, the dynamic logic is well-known in the art as used in Lee's invention. Lee discloses the dynamic logics (abstract) to compute a binary addition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the dynamic logic as disclosed in Lee's invention into Suzuki's invention because it would enable to reduce the power consumption and increase the system performance.

9. Claims 6-9, 11-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being obvious by Jiang et al. (U.S. 5,943,251) in view of Lee (U.S. 5,905,667).

Re claim 6, Jiang et al. disclose a N-bit parallel adder (col. 8 line 10) in Figure 7 comprising: a first logic stage configured to receive a first N-bit binary value and a second N-bit binary value and compute generate signals and propagate signals for each bit (P0G0-P35G35); a second logic stage coupled to the first logic stage (30-38) configured to compute block generate signal ($G^4_0 - G^4_8$) and block propagate signals ($P^4_0 - P^4_8$) for groups of one through m (m = 9) bits from the generate (G0-G35) and propagate (P0-P35) signals computed in the first logic stage; a third logic stage (40-42) coupled to the second logic stage (30-38) configured to combine the block generate and block propagate signals of one set of groups with the block generate ($G^{12}_0 - G^{12}_0$) and block propagate signals of another set of groups ($P^{12}_0 - P^{12}_0$); and a fourth logic stage (40) coupled to the third logic stage (40-42) configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal (Figure 8) wherein the

summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation (Figure 7 and equations 3-7 in col. 1), wherein at least one of the logic stages has dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Jiang does not disclose the adder is using a dynamic logic. However, the dynamic logic is well-known in the art as used in Lee's invention Figures 4-5. Lee discloses the dynamic logics (abstract) to compute a binary addition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the dynamic logic as disclosed in Lee's invention into Jiang's invention because it would enable to reduce the power consumption and increase the system performance (col. 3 lines 49-56).

Re claim 7, Jiang et al. further disclose a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i (col. 2 line 43), wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$ where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i (col. 1 equation 1) where a represents the first binary value and b represents the second binary value, and where p represents the propagate signal (col. 1 equation 2) and is equivalent to a logical summation operation between a_i and b_i.

Re claim 8, Jiang et al. further disclose in Figure 7 the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals (equation 7 in col. 1 wherein Ci is in col. 2 line 43).

Re claim 9, Jiang et al. further discloses in Figure 7 the fourth logic stage implements an exclusive OR function to generate the summation signal (col. 4 lines 16-17).

Re claim 11, Jiang et al. further disclose N is equal to 64 (col. 8 line 10 N = 64).

Re claim 13, it is the method claim of claim 6. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 12, Jiang et al. do not disclose the logic stages are implemented with complementary metal oxide semiconductor components. However, Lee discloses in Figure 3 the logic stages are implemented with complementary metal oxide semiconductor components (31). Therefore, it would have been obvious to a person having ordinary skill in the prior art at the time the invention is made to implement the logic stages disclosed by Jiang et al. with complementary metal oxide semiconductor components because it would enable to generate the complemented signal for computing the sum of two or more binary numbers and reduce the power consumption (col. 1 lines 37-42).

Re claim 14, it is the method claim of claim 7. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 15, it is the method claim of claim 8. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 16, it is the method claim of claim 9. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 18, it is the method claim of claim 11. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 19, it is the method claim of claim 12. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claim 20, it is the device claim of claim 6. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 6.

Allowable Subject Matter

10. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments filed 05/03/2004 have been fully considered but they are not persuasive.

a. The applicant argues in page 3 2nd paragraph for claim 1 under 102(b) that Lee fails to disclose a circuit having dynamic logic without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

The examiner respectfully submits that Lee discloses in Figure 4 as prior art invention a circuit having dynamic logic having clocks applied to transistors. In addition, Figure 4 does not disclose any inversion signal of the clock (CLKB) that driving the dynamic nodes as applicant argued. Instead, the clock (CLKB) is

directly applied (no inverter in between) to the P-MOS and N-MOS transistors to drive one or more dynamic nodes associated with the dynamic logic as cited by the claim.

b. The applicant argues in pages 3-4 3rd paragraph for claim 1 under 103(a) that Suzuki is non-analogous art since it does not disclose a binary adder circuit having dynamic logic.

The examiner respectfully submits that the main different between the present application and the reference by Suzuki is the dynamic logic. However as cited and admitted in the previous office action, the dynamic logic is well-known in the art as used in Lee's invention, particularly Figures 4-5. Lee discloses the dynamic logics (abstract) to compute a binary addition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the dynamic logic as disclosed in Lee's invention into Jiang's invention because it would enable to reduce the power consumption and increase the system performance (col. 3 lines 49-56).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

June 28, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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